

In the Claims

Please amend the claims as follows:

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1 1. (Currently Amended) The structure of a subpipelined
2 translation embodiment providing binary compatibility between a
3 base architecture and migrant architecture of a VLIW architecture
4 comprising:

5 a VLIW architecture comprising a base architecture and a
6 migrant architecture and having a base execution mode and a migrant
7 execution mode;

8 ~~a fetch packet retrieved~~ an instruction fetch unit for
9 simultaneously fetching from memory a group of a plurality of
10 instructions, each such group forming a fetch packet, the fetch
11 packet having an operating mode in dependence upon the execution
12 mode at the time the request was made to the memory for the fetch
13 packet;

14 a shared datapath by both the base and migrant architectures
15 for parsing said base architecture mode and migrant architecture
16 mode fetch packets into execute packets ~~and for dispatching those~~
17 ~~base execute packets to the appropriate base architecture decode of~~
18 ~~the execute hardware of~~ instructions within said fetch packet that
19 can be executed simultaneously;

20 a base architecture control circuit for dispatching execute
21 packet instructions having a base execution mode;

22 a migrant architecture control circuit for dispatching execute
23 packet instructions having a migrant execution mode ~~to a migrant~~
24 ~~architecture decode;~~

25 a base architecture decode connected to said shared datapath
26 and said base architecture control circuit for decoding an execute
27 packet in said base mode and generating a corresponding machine
28 word;

29 a migrant architecture decode connected to said shared
30 datapath and said migrant architecture control circuit for decoding
31 an execute packet in said migrant mode and generating a
32 corresponding machine word;

33 ~~execute hardware for executing execute packet instructions on~~
34 ~~execution units and having a base architecture decode and a migrant~~
35 ~~architecture decode for decoding said base architecture~~
36 ~~instructions and said migrant architecture instructions,~~
37 ~~respectively, in dependence upon the execution mode of the fetch~~
38 ~~packet of the instructions being decoded, prior to executing;~~

39 a multiplexer having at least two inputs and one machine word
40 output wherein one input is the machine word output of said migrant
41 architecture decode and the other input is the machine word output
42 of said base architecture decode, said multiplexer choosing in
43 dependence upon the operating mode of said fetch packet; and

44 ~~machine words for controlling the execution hardware units~~
45 execute hardware connected to said multiplexer for executing
46 execute packet instructions on execution units corresponding to
47 said machine word chosen by said multiplexer.

1 2. (Currently Amended) The structure according to Claim 1,
2 and further comprising a third input to said multiplexer wherein
3 said third input is a no operation instruction machine word.

1 3. (Original) The structure according to Claim 1, wherein
2 said machine word also controls registers.

1 4. (Original) The structure according to Claim 1, wherein said
2 machine word controls a global register file, which supplies
3 operands to all hardware execution units and accepts results of all
4 hardware execution units.

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1 5. (Original) The structure according to Claim 4, wherein
2 said machine word controls local register files that supply
3 operands to either local execution hardware functional units or
4 neighbor hardware execution functional units subsequent to said
5 machine word controlling said global register file.

1 6. (Original) The structure according Claim 5, wherein said
2 machine word controls the various types of execution hardware that
3 evaluate functions on the operands to produce the results of said
4 hardware execution units subsequent to said machine word
5 controlling said local register files.

1 7. (Original) The structure according to Claim 1, wherein the
2 base and migrant architecture decode units translates opcodes to
3 the control signals required to execute the specified instructions
4 on the execution hardware functional units.

1 8. (Original) The structure according to claim 1, and further
2 comprising said migrant architecture control circuit for issuing
3 no-operation instruction to preserve the semantics of the
4 instruction in the migrant architecture.

1 9. (Original) The structure according to Claim 1, wherein
2 said VLIW architecture is a Digital signal Processor (DSP).

1 10. (Currently Amended) A method of providing binary
2 compatibility between a base architecture and migrant architecture
3 of a VLIW architecture comprising the steps of:

4 ~~executing a base execution mode and a migrant execution mode~~
5 ~~on a base architecture and a migrant architecture, respectively, on~~
6 ~~a VLIW architecture,~~

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7 ~~providing a fetch packet retrieved simultaneously fetching~~
8 ~~from a memory a group of a plurality of instructions, each such~~
9 ~~group forming a fetch packet, the fetch packet having an operating~~
10 ~~mode in dependence upon the execution mode at the time the request~~
11 ~~was made to the memory for the fetch packet;~~

12 ~~parsing said base architecture mode and migrant architecture~~
13 ~~mode fetch packets into execute packets and dispatching those base~~
14 ~~execute packets to the appropriate base architecture decode of the~~
15 ~~execute hardware on a shared datapath by both the base and migrant~~
16 ~~architectures of instructions within said fetch packet that can be~~
17 ~~executed simultaneously;~~

18 ~~dispatching execute packet instructions having a base~~
19 ~~execution mode;~~

20 ~~dispatching execute packet instructions having a migrant~~
21 ~~execution mode to a migrant architecture decode on a migrant~~
22 ~~architecture control circuit;~~

23 ~~decoding an execute packet in said base mode and generating a~~
24 ~~corresponding machine word;~~

25 ~~decoding an execute packet in said migrant mode and generating~~
26 ~~a corresponding machine word;~~

27 ~~executing execute packet instructions on execution units of~~
28 ~~execute hardware said execute hardware having a base architecture~~
29 ~~decode and a migrant architecture decode for decoding said base~~
30 ~~architecture instructions and said migrant architecture~~
31 ~~instructions, respectively, in dependence upon the execution mode~~
32 ~~of the fetch packet of the instructions being decoded, prior to~~
33 ~~executing;~~

34 ~~choosing one machine word output, in dependence upon the~~
35 ~~operating mode of said fetch packet, between the output of machine~~
36 ~~word decoded in said migrant architecture decode mode and the~~
37 ~~output of machine word decoded in said base architecture decode in~~
38 ~~a multiplexer having one machine word output mode;~~

39 controlling the execution hardware units with said chosen
40 machine word.

1 11. (Currently Amended) The method according to Claim 10, and
2 further comprising choosing between the output of said migrant
3 architecture decode and the output of said base architecture decode
4 input and a no operation ~~instruction~~ machine word.

1 12. (Original) The method according to Claim 10, and further
2 comprising controlling registers with said machine word.

1 13. (Original) The method according to Claim 10, and further
2 comprising controlling a global register file with said machine
3 word, which supplies operands to all hardware execution units and
4 accepts results of all hardware execution units.

1 14. (Original) The structure according to Claim 13, and
2 further comprising controlling local register files that supply
3 operands to either local execution hardware functional units or
4 neighbor hardware execution functional units subsequent to said
5 controlling said global register file.

1 15. (Original) The method according Claim 14, and further
2 comprising controlling the various types of execution hardware that
3 evaluate functions on the operands to produce the results of said
4 hardware execution units subsequent to controlling said local
5 register files.

1 16. (Original) The method according to Claim 10, and further
2 comprising translating opcodes to the control signals required to
3 execute the specified instructions on the execution hardware

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4 functional units within the base and migrant architecture decode
5 units.

1 17. (Original) The method according to claim 10, wherein said
2 VLIW architecture is a Digital Signal Processor (DSP).

1 18. (Original) The method according to Claim 10 and further
2 comprising the step of issuing no-operation instruction from said
3 migrant architecture control circuit, to preserve the semantics of
4 the instructions in the migrant architecture.